DETAILED ACTION

Priority

1. Examiner acknowledged that this application 10/594,116 filed on 08/07/07 claims the benefit of the foreign application JP 2004-092982 filed on 03/26/04.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Honda (US PGPUB 2001/0026021 A1) and Saito (US Patent No. 6,573,739 B1).

6. As to claims 1, 13, and 18, Honda discloses:

(a) forming ordinary interconnections (electrode 2, Figs. 5A-7A) **on a first major surface of a wafer** (upper surface of substrate 1, Figs. 5A-7A)**; (b) forming re-interconnections** (layers 7, 8, and 11, Figs. 7B-9A) **including plural first metal film regions** (layers 11b, 8 and 7 below electrode 15 as shown in Fig. 11A) **and plural second metal film regions over the ordinary interconnections** (layers 7, 8, and 11 above electrode 2 as shown in Fig. 9A)**; (c) forming a polymeric resin film over the re-interconnections** (photoresist film 13, Fig. 9B)**; (d) forming plural first metal pad regions** (electrode 15, Fig. 10A) **by forming openings through portions of the polymeric resin film** (openings 14, Fig. 9C) **which correspond to the first metal film regions by a lithography technique** (Figs. 9B-10B; col. 5, [0065]-[0068]) **and "forming plural second metal pad regions"** (layer 30 and support plate 17, Fig. 15)**; (e) forming bumps on the respective first metal pad regions** (solder bump 16, Fig. 12A)**; (f) after the step (e), dividing the wafer into plural semiconductor integrated circuit chips** (Figs. 14-15) **[claim 1];**

However, Honda fails to disclose:

"the plural second metal pad regions" are formed by forming openings through portion of the polymeric resin film which correspond to the second metal film regions by a lithography technique [claim 1];

However, it would have been an obvious modification to the method disclosed by Honda because Honda discloses the first metal pad regions are formed by forming openings through portion of the polymeric resin film which correspond to the first metal film regions by a lithography technique and a person with ordinary skill in the art at time of the invention would have readily recognized that such technique is capable of forming additional pad regions at the desire locations and employ such technique in order to form second pad regions.

Although Honda discloses substantial features of the claimed invention (see paragraphs above), it fails to disclose:

using a bump formation surface, corresponding to the first major surface of the wafer, of a first semiconductor integrated circuit chip among the plural divisional semiconductor integrated circuit chips to be opposed to an electrode surface of a burn-in test socket, and performing a burn-in test in a state that the plural bumps on the bump formation surface and plural metal projection electrodes on the electrode surface are pressed against each other; and (h) after the step (g), separating the metal projection electrodes and the bumps of the first semiconductor integrated circuit chip from each other by pushing at least one of the plural second metal pad regions on the bump formation surface in such a direction that the first semiconductor integrated circuit chip and the electrode surface go away from each other by bringing at least one pushing member whose contact surface is narrower than the at least one second metal pad region into contact with the at least one second metal pad region [claim 1];

where at least one second metal pad region in the first semiconductor integrated circuit chip is in an electrically floating state [claim 13];

where the at least one pushing member is not brought into contact with a top surface of the polymeric resin film [claim 18].

Nonetheless, these features are well known in the art and would have been an obvious modification of the method disclosed by Honda, as evidenced by Saito.

Saito discloses:

using a bump formation surface, corresponding to the first major surface of the wafer, of a first semiconductor integrated circuit chip among the plural divisional semiconductor integrated circuit chips (the bottom surface of IC, Fig. 10) **to be opposed to an electrode surface** (the surface that the contact pins 51 are sitting on as shown in Fig. 10) **of a "test socket"** (socket guide 40, Fig. 10)**, and performing a "test" in a state that the plural bumps on the bump formation surface and plural metal projection electrodes on the electrode surface are pressed against each other (**col. 8, line 65 to col. 9, line 3)**; (h) after the step (g), separating the metal projection electrodes and the bumps of the first semiconductor integrated circuit chip from each other by pushing at least one of the plural second metal pad regions on the bump formation surface in such a direction that the first semiconductor integrated circuit chip and the electrode surface go away from each other** IC (the IC have to be pushed up by insert 16 after testing/Fig. 11 in order transport the IC to a different area for further processing such as encapsulation and mounting on a printed circuit board) **by bringing at least one pushing member** (the

bottom plate of holder 19 as shown in Fig. 10) **whose contact surface** (the upper surface of the bottom plate as shown in Fig. 10) **is narrower than the at least one second metal pad region** (already disclosed in Honda, see layer 30 and support plate 17, Fig. 15) **into contact with the at least one second metal pad region** (layer 30 and support plate 17a, Fig. 15) **[claim 1];**

where at least one second metal pad region in the first semiconductor integrated circuit chip is in an electrically floating state (Fig. 10; since IC is in floating state, the second metal pad region in the IC is also in floating state) **[claim 13];**

where the at least one pushing member is not brought into contact with a top surface of the polymeric resin film (one of the bottom plates of holder 19 in Fig. 10 is in contact with the layer 30, not resin layer 20, in Fig. 15 of Honda when the IC is placed in the holder 19) **[claim 18].**

Given the teaching of Saito, a person having ordinary skill in the art at the time of the invention would have readily recognized the desirability and advantages of modifying Honda by employing the well known or conventional features of IC testing apparatus for a burn-in test or other IC related tests, in order to position the solder bump and the contact pins with higher accuracy for the purpose of making better contact and remove the IC from the test socket after the testing.

7. As to claims 2-5, 7, 9-11, and 12, Honda also discloses:

where the polymeric resin film contains a thermosetting resin, heat-resistant thermosetting resin, polyimide resin, or organic thermosetting resin, as a main component (col. 5, [0074]; col. 6, [0085], [0088]) **[claim 2-5];**

where the bumps are formed by a lithography technique or a printing technique (col. 5, [0071]; both lithography and printing technique are conventional) **[claim 7];**

where the number of at least one second metal pad region in the first semiconductor integrated circuit chip is two/three or more (the right, middle, and the left layers 30 and support plates 17a, Fig. 15) **[claims 9 and 10];**

where the at least one second metal pad region in the first semiconductor integrated circuit chip is provided in a chip peripheral/corner portion of the bump formation surface of the first semiconductor integrated circuit chip (layer 30 and support plate 17, Fig. 12B) **[claims 11 and 12].**

8. As to claims 6 and 8, although Honda in view of Saito discloses substantial features of the claimed invention (see paragraphs above), it fails to disclose:

where a pitch of the bumps is smaller than 500um [claim 6];

where a ratio of a height to a diameter of the bumps in terms of an average ratio of completed bumps in the chip is smaller than 60% [claim 8].

However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to form semiconductor integrated circuit chips, since it has

been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In *re Boesche*, 617 F2. 2d 272, 205 USPQ 215 (CCPA 1980).

9. As to claims 14-17, although Honda in view of Saito discloses substantial features of the claimed invention (see paragraphs above), it fails to disclose:

where an area of each of the second metal pad regions is two/three times or more larger than that of each of the first metal pad regions [claims 14-16];

where an area of the contact surface of each of the at least one pushing member is two times or more larger than that of each of the first metal pad regions [claim 17].

However, it would have been obvious to one having ordinary skill in the art the time the invention was made to form semiconductor integrated circuit chips, since it is well known that larger push area (the interface between the second metal pad region and the pushing member) would facilitate pushing up the IC easier after the testing and also reduce the force applied to push up the IC from reaching the internal components to prevent damage because larger area could spread out the force applied.

10. Claims 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Honda in view of Saito as applied to claim 1, and further in view of Masuda (US Patent No. 6,518,781 B2)

11. As to claims 19 and 20, although Honda in view of Saito discloses substantial features of the claimed invention (see paragraphs above), it fails to disclose:

where each of the metal projection electrodes is formed by forming a plating layer having gold as a main component on a core member having nickel as a main component [claim 19];

where each of the metal projection electrodes is formed by further plating, with rhodium, the plating layer having gold as the main component [claim 20].

Nonetheless, these features are well known in the art and would have been an obvious modification to the method disclosed by Honda in view of Saito, as evidenced by Masuda.

Masuda discloses:

where each of the metal projection electrodes is formed by forming a plating layer having gold as a main component on a core member having nickel as a main component (col. 9, lines 25-30) **[claim 19];**

where each of the metal projection electrodes is formed by further plating, with rhodium, the plating layer having gold as the main component (col. 9, lines 25-30) **[claim 20].**

Given the teaching of Masuda, a person having ordinary skill in the art at the time of the invention would have readily recognized the desirability and advantages of modifying Honda in view of Saito by employing the well known or conventional features of using nickel as the core and plate it with gold and rhodium, such as disclosed by Masuda, in order to reduce contact resistance in a heated state after a period of time.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ming Hung Hung whose telephone number is (571) 270-3832. The examiner can normally be reached on Monday through Friday 7:30AM-5:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha Nguyen can be reached on (571) 272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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